REQUESTED BY EXAMINER

In the claims

Please amend the claims as follows:

1. (Previously Presented) A memory system comprising:

an array of addressable storage elements arranged in a plurality of rows and a plurality of columns, wherein the array of addressable storage elements comprises a plurality of nonvolatile memory cells; and

decoding circuitry coupled to the array of addressable storage elements, the decoding circuitry, responsive to decoding a first element address, to access a first storage element of a first row of the plurality of rows, and the decoding circuitry, responsive to decoding a second element address consecutive to the first element address, to access a second storage element of a second row of the plurality of rows, the second row of the plurality of rows different from the first row of the plurality of rows;

wherein the first address comprises a group of bits;

wherein the second address comprises a group of bits;

wherein the decoding circuitry includes a row decoder and a column decoder;

wherein the row decoder is operable responsive to a first portion of the group of bits of the first address and the second address;

wherein the column decoder is operable responsive to a second portion of the group of bits of the first address and the second address, wherein a bit of the second portion is more significant than a bit of the first portion.

2. (Original) A memory system according to claim 1 wherein each of the storage elements stores one bit.

3. (Original) A memory system according to claim 1 wherein each of the storage elements stores a plurality of bits arranged as a word.

4. (Original) A memory system according to claim 1 wherein each of the storage elements stores a plurality of bits arranged as a page.

5. (Canceled).

6. (Currently Amended) A memory system comprising:

an array of storage elements arranged in a plurality of rows and a plurality of columns, each of the storage elements comprising an input and an output, each of the storage elements corresponding to a numeric address comprising more significant bits and less significant bits, wherein the array of storage elements comprises a plurality of nonvolatile memory cells;

decoder circuitry operable responsive to a plurality of numeric addresses, including a first numeric address and a second numeric address, the second numeric address consecutive to the first numeric address, the decoder circuitry including:

a column decoder coupled to the outputs of the storage elements of each of the plurality of columns, the column decoder operable responsive to at least one of the more significant bits, the column decoder operable responsive to a portion of the first numeric address and a portion of the second numeric address; and

a row decoder coupled to the inputs of the storage elements of each of the plurality of rows, the row decoder operable responsive to at least one of the less significant bits, the row decoder operable responsive to a portion of the first numeric address and a portion of the second numeric address.

7. (Original) A memory system according to claim 6 wherein

the input of each of the storage elements is a control gate, and

the output of each of the storage elements is a drain.

8. (Original) A memory system according to claim 6 wherein each of the storage elements stores one bit.

9. (Original) A memory system according to claim 6 wherein each of the storage elements stores a plurality of bits arranged as a word.

10. (Original) A memory system according to claim 6 wherein each of the storage elements stores a plurality of bits arranged as a page.

11. (Canceled)

12. (Original) A memory system according to claim 6 wherein each of the plurality of nonvolatile memory cells comprises a floating gate-type cell.

13. (Original) A memory system according to claim 6 wherein the at least one of the less significant bits comprises all of the less significant bits.

14. (Previously Presented) An embedded control system comprising:

a processor; and

a memory system coupled to the processor, the memory system comprising an input to receive an address signal from the processor, an output to send addressed information to the processor, and a plurality of blocks, each of the plurality of blocks comprising:

an array of nonvolatile memory cells arranged in a plurality of rows and a plurality of columns to store information within a plurality of pages, each of the plurality of pages comprising a plurality of words, each of the plurality of words comprising a plurality of bits; and

decoding circuitry comprising a column decoder and a row decoder, the decoding circuitry coupled to the input, the output and the array of nonvolatile memory cells, the decoding circuitry, responsive to the address signal having a first page address, accessing a first page of a first row of the plurality of rows, the decoding circuitry, responsive to the address signal having a second page address consecutive to the first page address, accessing a second page of a second row of

the plurality of rows, and, thereafter, the decoding circuitry coupling the first and second pages to the output;

wherein each address comprises a group of bits;

wherein the row decoder is operable responsive to a first portion of the group of bits;

wherein the column decoder is operable responsive to a second portion of the group of bits, wherein a bit of the second portion is more significant than a bit of the first portion.

15. (Previously Presented) An embedded control system comprising:

a processor; and

a memory system coupled to the processor, the memory system comprising an input to receive an address signal from the processor, an output to send addressed information to the processor, and a plurality of blocks, each of the plurality of blocks comprising:

an array of nonvolatile memory cells arranged in a plurality of rows and a plurality of columns to store information within a plurality of pages, each of the plurality of pages comprising a plurality of words, each of the plurality of words comprising a plurality of bits; and

decoding circuitry comprising a column decoder and a row decoder, the decoding circuitry coupled to the input, the output and the array of nonvolatile memory cells, the decoding circuitry, responsive to the address signal having a first page address, accessing a first page of a first row of the plurality of rows, the decoding circuitry, responsive to the address signal having a second page address consecutive to the first page address, accessing a second page of a second row of the plurality of rows, and, thereafter, the decoding circuitry coupling the first and second pages to the output;

wherein the address signal comprises:

least significant bits representative of addresses of bits within a word,

next least significant bits representative of addresses of words within a page,

intermediate significant bits representative of addresses of the plurality of rows, the intermediate significant bits more significant than the next least significant bits,

more significant bits representative of addresses of pages within the plurality of rows, the more significant bits more significant than the intermediate significant bits, and

next more significant bits representative of addresses of the plurality of blocks, the next more significant bits more significant than the more significant bits.

16. (Previously Presented) A method of accessing a memory system, the memory system comprising an array of addressable storage elements arranged in a plurality of rows and a plurality of columns, wherein the array of addressable storage elements comprises a plurality of nonvolatile memory cells, the method comprising:

decoding a first element address;

accessing, responsive to the first element address, a first storage element of a first row of the plurality of rows;

decoding a second element address, the second element address consecutive to the first element address; and

accessing, responsive to the second element address, a second storage element of a second row of the plurality of rows, the second row of the plurality of rows different from the first row of the plurality of rows;

wherein the first element address includes a group of bits;

wherein the decoding the first element address further includes decoding a first portion of the group of bits by a row decoder and decoding a second portion of the group of bits by a column decoder;

wherein a bit of the second portion is more significant than a bit of the first portion.

17. (Original) A method according to claim 16 wherein accessing a first storage element comprises reading a first page, the first page comprising a plurality of bits.

18. (Original) A method according to claim 17 wherein accessing a second storage element comprises reading a second page different from the first page, the second page comprising a plurality of bits.

19. (Original) A method according to claim 16 wherein accessing a first storage element comprises initiating a first burst access, the first burst access comprising a plurality of bits.

20. (Original) A method according to claim 19 wherein accessing a second storage element comprises initiating a second burst access different from the first burst access, the second burst access comprising a plurality of bits.

21. (Previously Presented) The memory system of claim 6 wherein:
the numeric address comprises a group of bits;
the row decoder is operable responsive to a first portion of the group of bits;
the column decoder is operable responsive to a second portion of the group of bits, wherein each bit of the second portion is more significant than a least significant bit of the first portion.

22. (Previously Presented) An embedded control system comprising:
a processor; and
a memory system coupled to the processor, the memory system comprising an input to receive an address signal from the processor, an output to send addressed information to the processor, and a plurality of blocks, each of the plurality of blocks comprising:
an array of nonvolatile memory cells arranged in a plurality of rows and a plurality of columns to store information within a plurality of pages, each of the plurality of pages comprising a plurality of words, each of the plurality of words comprising a plurality of bits; and
decoding circuitry comprising a column decoder and a row decoder, the decoding circuitry coupled to the input, the output and the array of nonvolatile memory

cells, the decoding circuitry, responsive to the address signal having a first page address, accessing a first page of a first row of the plurality of rows, the decoding circuitry, responsive to the address signal having a second page address consecutive to the first page address, accessing a second page of a second row of the plurality of rows, and, thereafter, the decoding circuitry coupling the first and second pages to the output;

wherein:

the address signal comprises a group of bits;

the row decoder is operable responsive to a first portion of the group of bits;

the column decoder is operable responsive to a second portion of the group of bits, wherein each bit of the second portion is more significant than a least significant bit of the first portion.

23. (Previously Presented) The memory system of claim 1 wherein each bit of the second portion is more significant than a least significant bit of the first portion.

24. (Previously Presented) The method of claim 16 wherein each bit of the second portion is more significant than a least significant bit of the first portion.

25. (Previously Presented) A memory system comprising an input to receive an address signal, an output to send addressed information, and a plurality of blocks, each of the plurality of blocks comprising:

an array of nonvolatile memory cells arranged in a plurality of rows and a plurality of columns to store information within a plurality of pages, each of the plurality of pages comprising a plurality of words, each of the plurality of words comprising a plurality of bits; and

decoding circuitry comprising a column decoder and a row decoder, the decoding circuitry coupled to the input, the output and the array of nonvolatile memory cells, the decoding circuitry, responsive to the address signal having a first page address, accessing a first page of a first row of the plurality of rows, the decoding circuitry, responsive to the address signal having a second page address

consecutive to the first page address, accessing a second page of a second row of the plurality of rows, and, thereafter, the decoding circuitry coupling the first and second pages to the output;

wherein the address signal comprises:

a first group of bits representative of addresses of the plurality of rows,

a second group of bits representative of addresses of pages within the plurality of rows, wherein the second group includes a bit more significant than a bit of the first group;

a third group of at least one bit representative of addresses of the plurality of blocks.

26. (Previously Presented) The embedded control system of claim 14, wherein at least one bit of the group of bits is representative of addresses of the plurality of blocks.

27. (Previously Presented) A memory system according to claim 1 wherein each of the plurality of nonvolatile memory cells comprises a floating gate-type cell.

28. (Previously Presented) A memory system according to claim 1 wherein each of the plurality of nonvolatile memory cells comprises an EEPROM cell.

29. (Previously Presented) A memory system according to claim 6 wherein each of the plurality of nonvolatile memory cells comprises an EEPROM cell.

30. (Previously Presented) An embedded control system according to claim 14 wherein each memory cell of the array of nonvolatile memory cells comprises a floating gate-type cell.

31. (Previously Presented) An embedded control system according to claim 14 wherein each memory cell of the array of nonvolatile memory cells comprises an EEPROM cell.

32. (Previously Presented) A method according to claim 16 wherein each of the plurality of nonvolatile memory cells comprises a floating gate-type cell.

33. (Previously Presented) A method according to claim 16 wherein each of the plurality of nonvolatile memory cells comprises an EEPROM cell.

34. (Previously Presented) An embedded control system according to claim 22 wherein each memory cell of the array of nonvolatile memory cells comprises a floating gate-type cell.

35. (Previously Presented) An embedded control system according to claim 22 wherein each memory cell of the array of nonvolatile memory cells comprises an EEPROM cell.

36. (Previously Presented) A memory system according to claim 25 wherein each memory cell of the array of nonvolatile memory cells comprises a floating gate-type cell.

37. (Previously Presented) A memory system according to claim 25 wherein each memory cell of the array of nonvolatile memory cells comprises an EEPROM cell.